

NFP-3200 NETWORK FLOW PROCESSOR

NETRONOME®

Overview and Benefits

For designers of communications equipment whose network processing requirements extend beyond simple forwarding, Netronome's Network Flow Processors deliver high-performance packet processing with intelligence, security and virtualization for millions of simultaneous flows.

Unlike network processors and multicore CPUs that lack L4-L7 programmability or cannot scale to 10 Gbps and beyond, Netronome's flow processors are powered by 40 programmable networking cores that deliver 2,000 instructions and 50 flow operations per packet at 30 million pps, enabling 20 Gbps of L2-L7 processing with line-rate security and I/O virtualization.

Product Highlights

- Source-code compatibility (including backwards-compatibility) with Intel® IXP28XX microengines for customer application migration
- High-performance solution with low power consumption for a broad range of L2-L7 applications, delivering up to 30 Mpps/20 Gbps packet forwarding, policing, scheduling, queue management and protocol interworking and 70-million enqueue/dequeue packet operations per second, enabling deep packet processing of 64-byte Ethernet packets with no loss of performance
- Enhanced microengine (v2.7) derived from the latest Intel version (v2.6); 40 separate microengines with eight threads each running up to 1.4GHz.
- High-performance 32-bit ARM11, plus L2 cache, for processing complex algorithms, route table maintenance, control plane and system-level management functions
- Two DDR3 DRAM interfaces support more than 70 Gbps of total bandwidth
- High-performance SRAM supports more than 300 MQOps (queuing operations/second)
- High-speed PCIe 2.0 interface to multicore x86 or external control plane processor
- Standards-based interfaces for easy integration (e.g., QDRII, DDR3, PCIe 2.0, XAUI, Interlaken)

- Packet and content processing with robust security features in a single component reduces system cost by eliminating need for multiple devices. Integrated cryptography engines provide hardware acceleration of multiple algorithms (including all currently standardized AES variants) performing IPsec encryption/decryption at up to 20 Gbps
- Fully programmable network processor architecture enables optimization of additional algorithms and protocols to support IPsec, TCP and SSL application environments



NFP-3200 Upgrades Over the IXP28XX

16 microengines (v2.5) upgraded to 40 microengines (v2.7)

The additional 24 microengines more than doubles the processing capability while remaining code-compatible with the IXP28XX NPU. Version 2.7 of the microengine enables 16k of programmable control store by pairing NFP microengines, and adds both ECC protection on the control stores and parity on the registers and local memory.

RDRAM replaced with DDR3 DRAM

The DDR3 memory interface provides customers with a means to increase their overall memory capability (2x performance and 4x the capacity), while significantly reducing the system cost by a factor of 10.

PCI upgraded to PCIe 2.0 (eight lanes)

The PCIe interface enables customers to use the NFP-3200 product family in both control plane and data plane applications.

Four QDR SRAM channels are replaced with two physical QDR SRAM channels and two virtual QDR Channels

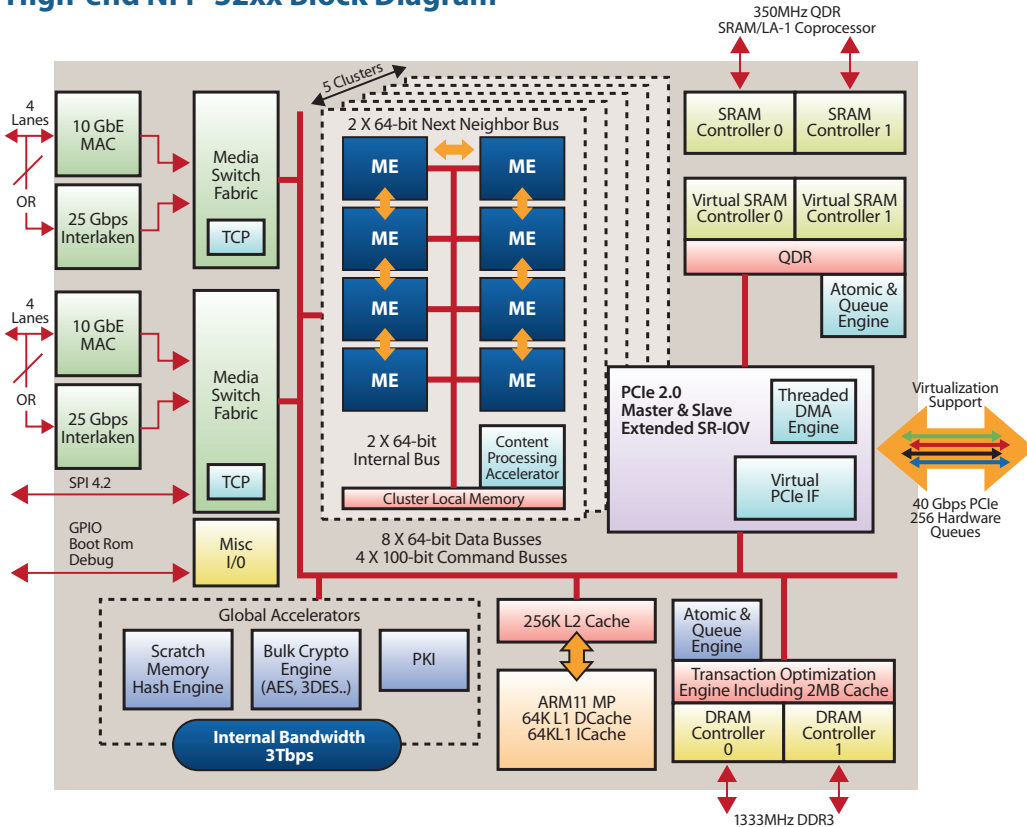
This change offers customers a higher-performance, lower-cost approach to attaining SRAM bandwidth, in terms of queuing operations (>5x performance increase). For applications requiring only two QDR SRAM Channels, no external parts are required.

The Netronome NFP family of network flow processors is the third-generation design of the industry's most popular network processing architecture. The NFP is built for high-performance network infrastructure designs that require high bandwidth, programmable data planes that span L2-L7 applications for carrier-grade and enterprise-class networking products, as well as virtualized networked servers and appliances. The NFP also extends the Intel® IXP28XX line of products, providing software source-code compatibility to protect existing software investments, while reducing system cost and enhancing available performance. Customers can easily migrate existing designs to this new generation of silicon and take advantage of improvements in performance, power consumption and price.



For more information about other Netronome products, please visit www.netronome.com.

High-end NFP-32xx Block Diagram



The integrated host Intel Xscale® Core is replaced by an ARM11 Core

The ARM11 Core has 256kB of L2 cache which increases the performance capabilities of the core.

A second Media Switch Fabric (MSF) interface has been added along with additional new features

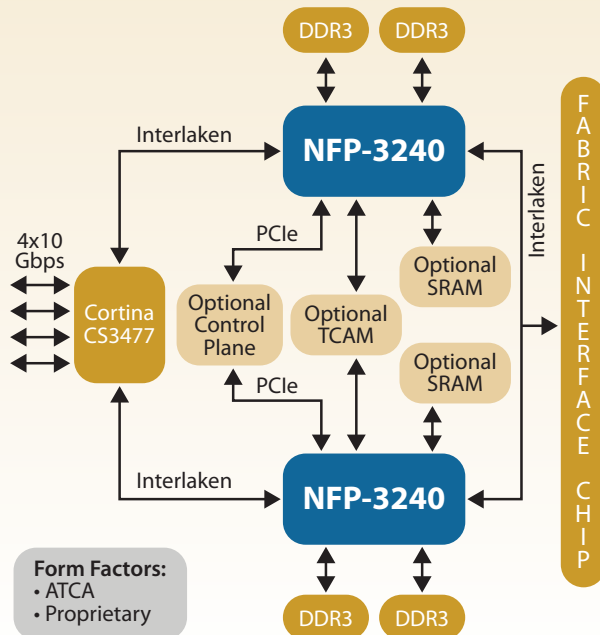
The second MSF Interface supports NFP usage in full-duplex configurations. The new features provide customers with a richer set of interface alternatives including XAUI (1x10 Gbps or 4x1 Gbps) or 4x6.25 Gbps lanes of Interlaken.

Features and Benefits of NFP-32xx

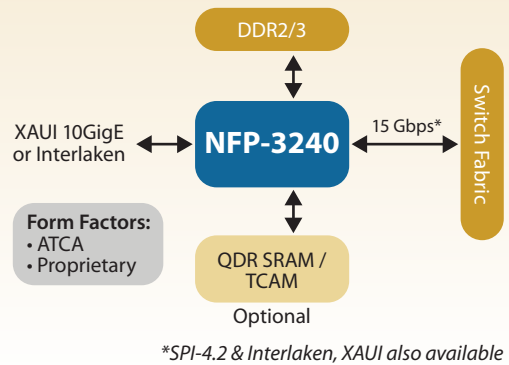
| FEATURES | BENEFITS |
|--|---|
| 40 microengines, each with eight threads and 8K-words of control store | High-performance, flexible, multi-threaded, RISC processor engines that are easily programmed for a variety of packet processing applications. Paired microengines provide 16k-word shared instruction stores for run-to-completion or pool-of-threads programming model. |
| Integrated ARM11, L1 cache (32-Kbyte instruction cache, 32-Kbyte data cache) plus L2 cache (256-Kbytes) | Embedded 32-bit RISC core for IKE, route table maintenance and system-level management function help to lower system cost and save board space. |
| Integrated PKI and cryptography blocks provide hardware acceleration for DES, 3DES, AES, SHA-1 and SHA-2 algorithms. | Enables bulk encryption/decryption for IPSec data streams at speeds up to 10 Gbps |
| Flow-through cryptography architecture processes packets "on-the-fly." | Increases performance and helps to minimize packet reassembly in memory. |
| Two programmable, unidirectional 16-bit LVDS data interfaces. One interface can be a single, bi-directional SPI-4 Phase 2, 1x10GbE MAC, 4x1GbE MAC or Interlaken interface. The other can be a single 1x10GbE MAC, 4x1GbE MAC or Interlaken interface. | Supports industry-standard interfaces to media and fabric devices, delivering greater than 10Gbps performance rate. Standard interface to I/O appliances, MACs/framers, and fabric interface chips. Standard interface supported by FPGA and ASIC vendors. |
| Two industry-standard DDR3 DRAM interfaces (two 64-bit) | High-density, high-bandwidth memory subsystem. Supports up to 8GByte of system DRAM memory. |
| DRAM-optimized cache | 2MB of internal cache, optimized to maximize the DDR performance and provide two additional "virtual QDR" channels |
| Two industry-standard 32-bit QDR SRAM interfaces | Multiple-channel, fast access to lookup tables, access lists, statistics and data structure control. Supports industry-standard NFP LA-1 interface for TCAM or look-aside processor additions. |
| PCIe 2.0 x8 I/O interface | Supports industry-standard connection to x86 or other control plane processors with PCIe 2.0 widths of up to eight lanes |
| Hardware support for memory access queuing | Simplifies memory queue structures and software support by utilizing internal hardware acceleration. |
| JTAG support | Standard board-level debug support. |
| Additional integrated hardware features: <ul style="list-style-type: none"> • Hardware hash unit (48-, 64-, and 128-bit) • 16-Kbyte scratchpad memory • Serial UART port for debug • 12 GPIO pins | Internal hardware structures for function acceleration, ring support and general-purpose utilization maximize software application options for efficiency and performance. |
| Software Development Kit and Hardware Development Kit | Shortens user development time |

Application Examples

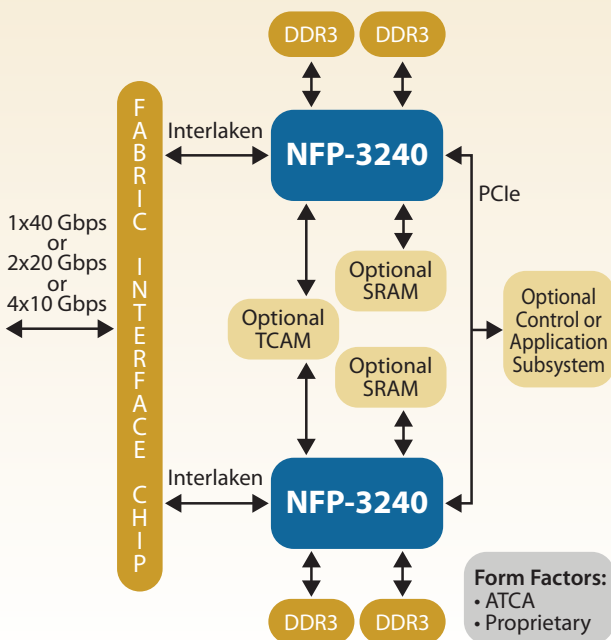
40 Gbps Programmable Line Card



Intelligent 10G Full-duplex Line Card



40 Gbps Programmable Service Blade



Specifications

Microengine v2.7 (8k instructions or 16k shared between 2 MEs; 1k-word local memory); 32-bit data path; up to 40 MEs and 320 threads; 56 billion instructions per second; 1800 instructions per packet and 1.84 billion instructions per watt.

| | |
|-------------------------------------|--|
| SPI-4 Phase 2 operation | 250-500MHz (622-1,000 MTs) |
| | 16-bit LVDS (dual-edge) signaling |
| XAUI interface | 3.125GHz for 4 lanes supporting 10 Gbps operation |
| Interlaken interface | 6.25GHz per lane (each of the 4 lanes supports 3.125-6.375GHz operation) |
| ARM11 core operating frequency | 700MHz, 500MHz and 325MHz/32-bit data path |
| GEN-II PCIe interface | Version 2, x8 (5.0 Gbps/lane, 40 Gbps total each way) |
| SRAM interface (QDR) (two channels) | Peak bandwidth of 2GBytes/sec per channel using 250MHz SRAMs (1GByte/sec Read, 1GByte/sec Write) |
| DDR3 DRAM (two channels) | Peak bandwidth 8.5GBytes/sec (68.2 Gbps) for 64-bit channel |
| Operating temp. | 0-70°C ambient |
| Power supply voltages | |
| ME Vdd Voltage | 1.125V±3% |
| ARM11 Core Vdd Voltage | 1.05V±3% |
| Memory I/O Voltage | 1.5V±5% |
| GEN-II PCIe I/O Voltage | 1.0V±3% |
| SPI4.2 I/O Voltage | 2.5V±5% |
| Interlaken Voltage | 1.0V±3% |
| Power dissipation | ~20W minimum, ~40W maximum across product family |
| Package | 1521 Ball FCBGA 1.57" (40 mm) × 1.57" (40 mm) |
| Solder ball pitch | 1 mm |

Product Availability

Netronome delivers a family of NFP-32xx Network Flow Processors to the market addressing various feature and performance points – from the NFP-3216 (16 MEs) to the NFP-3240 (40 MEs) – with all of them available in a RoHS-compliant 1521 FCBGA Package.

Also available from Netronome are supporting NFP Software Development Tools and an NFP-3200 Customer Development Platform.



The Flow Processing Company

Netronome has operations in:
USA (Pittsburgh [HQ], Santa Clara & Boston), UK (Cambridge), Malaysia (Penang), South Africa (Centurion) and China (Shenzhen, Hong Kong)

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