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The Flow Processing Company™

Netronome Discloses Processor Architecture Requirements for 100 Gbps Next Generation Firewall and OpenFlow Designs

Santa Clara, CA – October 4, 2011 – Netronome, the leading developer of network flow processors, today announced that Niel Viljoen, founder and chief development officer, will disclose new architecture requirements for processors being used in flow-based 100 Gbps communications designs, such as next-generation firewalls and OpenFlow switches and routers.

Mr. Viljoen's presentation will take place at The Linley Group's Tech Processor Conference, which focuses on networking and communications. The event is on October 5 and 6 at the Double Tree hotel in San Jose, California. Mr.Viljoen's presentation and panel session both take place on Thursday October 6, during Session 7, "100Gbps Networking."

"As the industry's foremost event focused exclusively on processors, The Linley Tech Processor Conference provides a forum for industry leaders to share the latest developments in processor and related technologies," said Joseph Byrne, an analyst with The Linley Group. "Netronome is a leader in flow processing solutions, and their insight on architectural requirements for processors targeting next-generation firewall and OpenFlow switching will be valuable information for our attendees."

Mr. Viljoen will discuss the use of high-performance, programmable, highly-threaded, many-core processors in communications designs that require stateful processing of millions of simultaneous flow at 100Gbps and beyond. Mr. Viljoen will focus on processor architectural considerations to enable high-bandwidth and low-latency access to memory, a key bottleneck in scaling L4-L7 designs to 100Gbps. Mr. Viljoen will also participate in a Q&A panel with executives from Radisys and Xelerated.

"New processor architecture must overcome many new challenges when trying to handle millions of flows at 100Gbp packet rates, specifically a multi-threaded approach that hides memory latency" said Mr. Viljoen. "Several challenges exist including on-chip memory optimization for increased access and reduced latency, recursive flow state lookups, and scalable access to packet data in local memory."

For more information about the Linley Tech Processor Conference, visit:
http://www.linleygroup.com/events/event.php?num=10.

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About Netronome
Netronome is a leading developer of highly programmable semiconductor products that are used for intelligent flow processing in network and communications devices. Netronome's solutions include network flow processors and acceleration cards that scale from 10 to 200 Gbps. They are used in carrier-grade and enterprise-class communications products that require deep packet inspection, flow analysis,

content processing, virtualization and security. Netronome's products are developed in labs in Santa Clara, CA, Boxborough, MA and Pittsburgh, PA. For more information on Netronome's products and technology, visit www.netronome.com.

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Media Inquiries:

Heather Fitzsimmons
Mindshare PR
On behalf of Netronome
Phone: 650.947.7400
Email: heather@mindsharepr.com

Jennifer Mendola
Marketing Communications Manager
Netronome
Phone: 724.778.3290
Email: jennifer.mendola@netronome.com