NETRONOME

PRODUCT BRIEF

Netronome NFP-32xxx

20 Gbps Programmable Flow Processors

Overview

For designers of virtualized data centers whose network processing requirements extend beyond simple forwarding, Netronome's Flow Processors deliver high-performance packet processing with intelligence, security and virtualization for millions of simultaneous flows.

Unlike network processors and multicore CPUs that lack L4-L7 programmability or cannot scale to 10 Gbps and beyond, Netronome's flow processors are powered by 40 programmable networking cores that deliver 2,000 instructions and 50 flow operations per packet at 30 million pps, enabling 20 Gbps of L2-L7 processing with security acceleration and I/O virtualization.

Netronome NFP-32xx Flow Processor Architectural Highlights

Features	Benefits
40 flow processing cores, each with eight threads and 8K to 16K words of control store	High-performance, flexible, multi-threaded, RISC processor engines that are easily programmed for a variety of packet processing applications.
Integrated ARM11 Core	Embedded 32-bit RISC core for IKE, route table maintenance and system-level management function help to lower system cost and save board space.
Integrated PKI and cryptography acceleration	Enables bulk encryption/decryption for IPSec data streams at speeds up to 10 Gbps
Two programmable, unidirectional data interfaces.	Supports industry-standard interfaces to media and fabric devices, delivering greater than 10 Gbps performance rate.
Two industry-standard DDR3 DRAM interfaces (two 64-bit)	High-density, high-bandwidth memory subsystem. Supports up to 8GByte of system DRAM memory.
DRAM-optimized cache	2MB of internal cache, optimized to maximize the DDR performance and provide two additional "virtual QDR" channels
Two industry-standard 32-bit QDR SRAM interfaces	Multiple-channel, fast access to lookup tables, access lists, statistics and data structure control. Supports industry-standard NPF LA-1 interface for TCAM or look-aside processor additions.
PCIe 2.0 x8 I/O interface	Supports industry-standard connection to x86 or other control plane processors with PCIe 2.0 widths of up to eight lanes
Hardware support for memory access queuing	Simplifies memory queue structures and software support by utilizing internal hardware acceleration.
JTAG support	Standard board-level debug support.
Software Development Kit and Hardware Development Kit	Shortens user development time

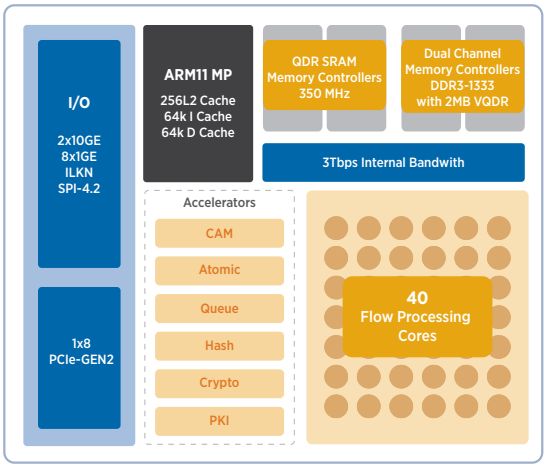
NETRONOME'S NFP-32XX

- Third generation family of flow processors
- Number one micro-architecture used in networking
- First fully programmable 40 Gbps L2-L7 processor
- First processor to combine packet and flow processing
- Only processor explicitly designed for flow co-processing

TARGET APPLICATIONS

- Intrusion Detection Systems (IDS) & Intrusion Prevention Systems (IPS)
- Next-Generation Firewalls (NGFW)
- Carrier SDN & NFV Appliances
- Open vSwitch (OVS) based platforms
- Data Center Virtualized Appliance
- Open Compute Platforms
- Test & Measurement Equipment
- Network Probes & Monitors
- Advanced Services Blades

NFP-32xx Flow Processor Block Diagram



Product Highlights

- High-performance solution with low power consumption for a broad range of L2-L7 applications, delivering up to 30 Mpps/20 Gbps packet forwarding, policing, scheduling, queue management and protocol interworking and 70-million enqueue/dequeue packet operations per second, enabling deep packet processing of 64-byte Ethernet packets with no loss of performance
- Packet and content processing with robust security features in a single component reduces system cost by eliminating need for multiple devices. Integrated cryptography engines provide hardware acceleration of multiple algorithms (including all currently standardized AES variants) performing IPSec encryption/decryption at up to 20 Gbps
- Fully programmable network processor architecture enables optimization of additional algorithms and protocols to support IPSec, TCP and SSL application environments
- High-performance 32-bit ARM11, plus L2 cache, for processing complex algorithms, route table maintenance, control plane and system-level management functions
- Two DDR3 DRAM interfaces support more than 70 Gbps of total bandwidth
- High-performance SRAM supports more than 300 MQOps (queuing operations/second)
- High-speed PCIe 2.0 interface to multicore x86 or external control plane processor
- Standards-based interfaces for easy integration (e.g., QDRII, DDR3, PCIe 2.0, XAUI, Interlaken)
- Source-code compatibility (including backwards-compatibility) with Intel® IXP28XX microengines for customer application migration

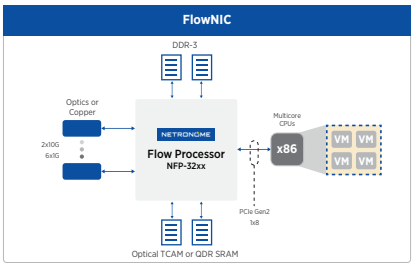
Specifications

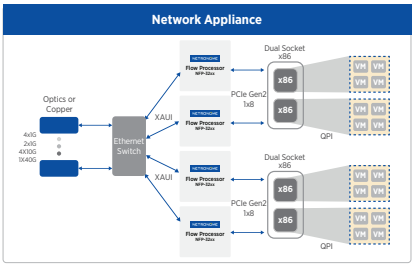
Flow Processing Cores ..... 40 FPCs, 320 threads, 32-bit data path (8k instructions or 16k shared between 2 FPCs)
SPI-4 Phase 2 Operation ..... 250-500MHz (622-1,000 MTs) 16-bit LVDS (dual-edge) signaling
XAUI Interface ..... 3.125GHz for 4 lanes supporting 10 Gbps operation
Interlaken Interface ..... 6.25GHz per lane (each of the 4 lanes supports 3.125-6.375GHz operation
ARM11 Core Operating Frequency ..... 700MHz, 500MHz and 325MHz/32-bit data path
PCIe Interface ..... Version 2, x8 (5.0 Gbps/lane, 40 Gbps total each way)
SRAM Interface (QDR) (two channels) ..... Peak bandwidth of 2GBytes/sec per channel using 250MHz SRAMs (1GByte/sec Read, 1GByte/sec Write)
DDR3 DRAM (two channels) ..... Up to 1333 MTs, peak bandwidth 8.5GBytes/sec (68.2 Gbps) for 64-bit channel
Operating Temperature ..... 0-70°C ambient

Power Supply Voltages

FPC Vdd Voltage ..... 1.125V±3%
ARM11 Core Vdd Voltage ..... 1.05V±3%
Memory I/O Voltage ..... 1.5V±5%
PCIe 2.0 I/O Voltage ..... 1.0V±3%
SPI4.2 I/O Voltage ..... 2.5V±5%
Interlaken Voltage ..... 1.0V±3%
Power Dissipation ..... ~20W min., ~40W max. across product family
Package ..... RoHS-Compliant 1521 Ball FCBGA 1.57" (40 mm) X 1.57" (40 mm)
Solder Ball Pitch ..... 1 mm

SAMPLE DESIGNS





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